Notice of Allowability	Application No.	Applicant(s)	
	10/796,331	MELTZER ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment - After Non-Final Rejection, filed 10/09/2007*.

2. ☒ The allowed claim(s) is/are *1-22*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Drawings

The modifications to the drawings were received on 10/09/2007. These modifications are accepted by the Examiner.

In view of the amendment filed on 10/09/2007, the Examiner withdraws drawings objections of the previous Office action.

Specification

The modifications to the specification were received on 10/09/2007. These modifications are accepted by the Examiner.

In view of the amendment filed on 10/09/2007, the Examiner withdraws specification objections of the previous Office action.

Claim Objections

The modifications to the claims were received on 10/09/2007. These modifications are accepted by the Examiner.

In view of the amendment filed on 10/09/2007, the Examiner withdraws claim objections to claims 1-22 of the previous Office action.

Response to Arguments

Applicant's arguments, see Amendment - After Non-Final Rejection, filed 10/09/2007, with respect to claim 1 has been fully considered and are persuasive. The rejection of claim 1 has been withdrawn.

Allowable Subject Matter

Claims 1-22 are allowed.

The following is an examiner's statement of reasons for allowance: claims 1-22 are allowed because a comprehensive search of prior art failed to teach, either alone or in combination, a frequency synthesizer comprising an input node for receiving a reference frequency signal, a variable oscillator having a first control input and a second control input, and producing an oscillator output signal whose frequency is dependent on the first and second control inputs, an analog voltage phase detector having a first phase-detection input responsive to the reference frequency signal and a second phase-detection input responsive to the oscillator output signal from the variable oscillator, the analog voltage phase detector being effective for producing a first control signal indicative of a phase difference between the reference frequency signal and the oscillator output signal, the first control signal being coupled to the first control input of the variable oscillator, where an analog loop is defined by the signal path along the first control signal from the analog voltage phase detector to the variable oscillator and along the oscillator output signal from the variable oscillator back to the analog voltage phase detector, a digital frequency difference detector having a first frequency-detection input responsive to the reference frequency signal and a second frequency-detection input responsive to the oscillator output signal, the digital frequency difference detector being effective for producing a second control signal indicative of a frequency difference between the reference frequency signal and the oscillator output signal, the second control signal being coupled to the second control input of the variable oscillator, where a digital loop is defined by the signal path along the second control signal from the digital frequency difference detector to the variable oscillator and along the oscillator

output signal from the variable oscillator back to the digital frequency detector, where the bandwidth of the analog loop is greater than the bandwidth of the digital loop; and a frequency synthesizer comprising an input node for receiving a reference frequency signal, a variable oscillator having a first control input and a second control input, and producing an oscillator output signal whose frequency is dependent on the first and second control inputs, an analog voltage phase detector having a first phase-detection input responsive to the reference frequency signal and a second phase-detection input responsive to the oscillator output signal from the variable oscillator, the analog voltage phase detector being effective for producing a first control signal indicative of a phase difference between the reference frequency signal and the oscillator output signal, the first control signal being coupled to the first control input of the variable oscillator, where an analog loop is defined by the signal path along the first control signal from the analog voltage phase detector to the variable oscillator and along the oscillator output signal from the variable oscillator back to the analog voltage phase detector, a digital frequency difference detector having a first frequency-detection input responsive to the reference frequency signal and a second frequency-detection input responsive to the oscillator output signal, the digital frequency difference detector being effective for producing a second control signal indicative of a frequency difference between the reference frequency signal and the oscillator output signal, the second control signal being coupled to the second control input of the variable oscillator, where a digital loop is defined by the signal path along the second control signal from the digital frequency difference detector to the variable oscillator and along the oscillator output signal from

the variable oscillator back to the digital frequency detector where the digital frequency difference detector includes an n-bit counter for counting pulses received at the first frequency-detection input, whereby the n-bit counter maintains a pulse-count of the reference frequency signal; an m-bit counter for counting pulses received at the second frequency detection input, whereby the m-bit counter maintains a pulse-count of the oscillation output signal, and where m is greater than n; a first memory cell for storing a SET condition in response to the nth bit within the m-bit counter transitioning into a first logic state and for maintaining the SET condition irrespective of the n^{th} bit within the m-bit counter transitioning out of the first logic state; a second memory cell for storing a SET condition in response to the $(n+1)^{th}$ bit within the m-bit counter transitioning into the first logic state and for maintaining the SET condition irrespective of the $(n+1)^{th}$ bit transitioning out of the first logic state; where the n-bit counter and the m-bit counter are halted in response to the n^{th} bit, within the n-bit counter transitioning into the first logic state; and where upon the halting of the n-bit and m-bit counters, the digital frequency difference detector determines a) that the output frequency of the variable oscillator is lower than the reference frequency signal when neither of the first or second memory cells have the SET condition stored; or b) that the output frequency of the variable oscillator is higher than the reference frequency signal when the second memory cell has the SET condition stored; or c) that the output frequency of the variable oscillator is higher than the reference frequency signal when the first memory cell has the SET condition stored and any bit within the m-bit counter excluding a predetermined number of least significant bits is set to the first logic state; or d) that the

output frequency of the variable oscillator is locked to the reference frequency signal when the first memory cell has the SET condition stored and the second memory cell does not have the SET condition stored and no bit within the m-bit counter excluding the predetermined number of least significant bits is set to the first logic state, as the applicant has claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is 571-272-3119. The examiner can normally be reached on 8-6 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Juan Alberto Torres
10-10-2007

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER